Dear 82C465MV Customer:

OPTi is now sampling 82C465MV/A silicon. Samples are identified by the date code of 9443RE on the chip. Some samples are marked as 82C465MV instead of 82C465MV/A, so the date code is the only reliable indication of revision A silicon.

Revision A silicon corrects flaws in the 82C465MV silicon, and also adds many new features as described in the "82C465MV/A Product Brief". The 82C465MV part will eventually be replaced completely by the 82C465MV/A part.

This memo calls attention to subtle differences between the 82C465MV part and the 82C465MV/A part that might at first make the parts appear to be incompatible. If there are any issues that are unclear in this memo, please contact Mark R. Williams at OPTi, (408) 486-8607.

There are two known areas to which proper attention must be directed.

LCLK Becomes BOFF#

The LCLK pin on the 82C463MV part, pin 189, was used to provide a 1X clock for the VL bus in case a 2X CPU was being used. This pin was maintained on the 82C465MV part only to ensure pin-compatibility with the 82C463MV, and is replaced by TAGCS# if L2 cache is used. The 82C465 series parts always generate a 1X clock on FBCLKOUT, regardless of whether a 1X or 2X CPU is used, and therefore have no need for LCLK.

To make better use of pin 189 on the 82C465MV/A part, the LCLK signal is automatically replaced by BOFF# for use by L1 writeback CPUs. The pin 189 function is determined at reset time depending on whether the following two conditions are true.

1. The 463-compatible interface mode of the chip is disabled, meaning that pin 79 must be strapped low (or not at all).

2. The L2 cache interface is disabled, meaning that pin 146 is strapped high (or not at all).

Under these conditions pin 189 becomes BOFF# at reset time. If LCLK is needed even in these circumstances, setting bit D4h[0]=1 restores pin 189 to its LCLK function.

Note: On 82C465MV/A sample silicon, date code 9443RE, bit D4h[0] is not yet implemented so the LCLK function cannot be restored. However, bit D4h[0] will be implemented in **all** production silicon.

RSVD Mux Phase Becomes ATHOLD

The C1 phase of the EPMMUX input (pin 88) is a "don't care" on the 82C465MV part. The demo board schematics indicate that this input must be tied low. This pin defaults to a DRQ2 input alone, and is only changed to a muxed input by programming. However, even if muxing is enabled but only DRQ2 is connected, the system will work properly because the other phases are all "don't cares" unless enabled.

On the 82C465MV/A part, this situation changes slightly. The C1 phase automatically becomes ATHOLD, a function which will prevent any future activity on the AT bus and also tri-state the bus in anticipation of a docking station attachment. If pin 88 is programmed as a muxed input but only DRQ2 is connected, the chip will tri-state the AT bus any time DRQ2 goes high.

Functional Improvements over 82C465MV Part

The following flaws in the 82C465MV part are corrected in the 82C465MV/A part.

1. DRAM operation is no longer limited to 4-3-3-3 read cycles when L2 cache is enabled as it was on the 82C465MV part; 3-2-2-2 operation is permitted if the system DRAM is capable of this speed. If the problem was corrected in hardware using the gating scheme suggested for the 82C465MV part, this external fix should be removed for the 82C465MV/A part.

2. L2 cache cycles now run at 2-1-1-1 if programmed on the 82C465MV/A part, as opposed to the 82C465MV part which ran 3-1-1-1 cycles either way. See also the Documentation Issues section below.

3. The 82C465MV chip internally does not qualify SMIACT# with HLDA, and so incorrectly remaps DMA transfers to SMM memory. The 82C465MV/A part qualifies SMIACT# properly with HLDA. The gate fix suggested for the 82C465MV part can be left on if present, but is no longer needed.

4. When the 82C465MV part was programmed to use the ATCLKIN input as source for ATCLK timing, hardware reset (RST1#) would fail on the first try. The 82C465MV/A part will reset properly regardless of ATCLKIN.

5. The DRAM controller of the 82C465MV part would wrap around in its decoding over 2GB. The 82C465MV/A part properly qualifies operations with A31, and no longer causes accesses above 2GB to wrap around to low memory.

Documentation Issues

The following issues refer to the 82C465MV Data Book revision 1.0, product code 912-3000-016.

1. There is a mistake in the 82C465MV Data book regarding cache programming. Bits D0h[2] and D0h[0] have their '0' and '1' settings reversed. The corrected version of the register is illustrated below. This is true for both the 82C465MV and 82C465MV/A silicon.

Index	Name	7	6	5	4	3	2	1	0
D0h	**L2 Cache Control Register 1**	L2 cache CCS0-3# deassert 0=stop grant and suspend 1=also btw. accesses	L2 cache controls state during suspend 0=tri-state 1=driven	L2 Cache Engage 0=Disable 1=Enable	Cache Size 0 0=64KB 0 1=128KB 1 0=256KB 1 1=reserved		**L2 Cache Write Wait State 0=1 ws 1=no ws**	L2 Cache Read Burst Wait State Control 0=X-1-1-1 1=X-2-2-2	**L2 Cache First Read Wait State Control 0=3-X-X-X 1=2-X-X-X**

2. In the Integrated Local-Bus Enhanced IDE Controller section of the data book, page 67, the figure illustrating IDE connections incorrectly shows an inverter on the HDCS0# line. The inverter should be on the HDCS1# line. This signal is derived from SA9 (put out on the TC pin for IDE cycles). HDCS0# is active for 1F0-1F7h cycles (SA9 low), and inactive for 3F6-3F7h cycles (SA9 high).

3. The channel 3 DMA count register on page 63 is at I/O address 007h, not 006h.

4. Pinout figures on pages 10, 12, 13, and 14 indicate VCC on pin 26; it should be VSS. Pin descriptions in the tables are correct, as is the schematic symbol in the demonstration board schematics file.