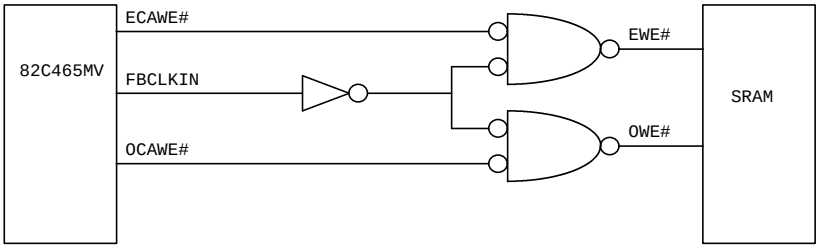
OPTi **Memo** **8 September 94**

To: 82C465MV Customers
From: Mark R. Williams, Tech. Mktg. Engineer (408) 486-8412
Subject: 82C465MV Errata

This memo summarizes the 82C465MV problems found up to now through the debug process. These problems will be corrected on the 82C465MV/A silicon, which will be in production late in Q4 of this year.

1. DRAM operation is limited to 4-3-3-3 read cycles whenever the L2 cache is enabled. This problem can be corrected in hardware using the scheme below that reduces the active time of the ECAWE# and OCAWE# signals to the SRAM. DRAM can be run at 3-2-2-2 when this fix is introduced.



2. L2 cache cycles can only run as fast as 3-1-1-1, even if 2-1-1-1 cycles are programmed. There is no external fix available for this problem.

3. DMA transfers can corrupt SMM memory space. When the chipset system is operating in SMM (SMIACT# active), a DMA transfer to or from a memory address location with the same segment as SMBASE will access SMM memory space, not the intended memory buffer in system DRAM. The 82C465MV chip does not internally qualify SMIACT# with HLDA and so incorrectly remaps DMA transfers to SMM memory. The fix for this problem is described in a separate Product Update and requires 1-2 gates depending on the system design.

4. When the 82C465MV chip has been programmed to use the ATCLKIN input as source for ATCLK timing, hardware reset (RST1#) fails on first try because the logic prevents ATCLK from restarting. If the RST1# input is pulsed a second time, the reset proceeds normally. There is currently no external fix for this problem.

5. The DRAM controller ignores A31, causing accesses above 2GB to wrap around to low memory. While this problem is minor, a side effect is that the DRAM write protect feature is disabled during this wraparound, leaving shadowed BIOS and SMM code vulnerable to memory writes made above 2GB. The fix for this problem is to connect A31 to the A25 input of the chip, limiting maximum addressable DRAM to 32MB.