OPTi Inc.
660 Alder Drive
Milpitas, CA 95035
Fax: (408) 382-2601
Phone: (408) 382-2600

Product Alert

Product Name: **FireLink 82C862 PCI-to-USB Bridge**

Title: **Clock Issue**

Date: **January 8, 2001**

Scope

This document provides information on a problem that has been identified with the OPTi 82C862 PCI-to-USB Bridge revision 0.2 when using its internal PLL. These chips are identified by a four-digit code of "02 ME" that is stamped on the top side of the chip.

Issue

Tracking No: 12498

When the 82C862 chip is used with its on-board PLL enabled, that is, when using an external 12MHz crystal, the internal 48MHz clock may not always be generated properly even though the PLL X1 and X2 pins are oscillating properly at 12MHz.

This problem can only occur when using an external 12MHz crystal and TEST1 is strapped low. If an external 48MHz can oscillator is used, and TEST1 is correspondingly strapped high, there is no problem.

This is a noise issue related to the way the strap is sampled when RESET# is low, and is seen on some (but not all) devices.

Workaround

A board level rework will eliminate the potential problem. The TEST1 strap option pin must be pulsed high and then brought low after power is stable but prior to the deassertion of RESET#.

Various methods can be employed to do this, but the simplest involves two capacitors and a resistor that act to generate a high pulse on TEST1 and at the same time delay RESET# to the chip.

The workaround is illustrated in Figure 1.

Fix

A silicon fix will be implemented at the next silicon revision opportunity. However, because the workaround provided is 100% effective in preventing the problem from occurring, there are currently no plans to revise the chip.

The workaround provided can be left in place even with the anticipated revised chip, and will not cause any problems.

Figure 1. Workaround Implementation